

WE CLAIM:

1. An error correction system, comprising:
  - an input buffer, connected to a first port;
  - a latch, connected to the input buffer, for latching data;
  - an edit buffer having an error portion for storing an error correction word and a data portion for storing a data word;
  - an error word generator having an input and an output, the input connected to the latch and the output connected to the edit buffer, for generating an error word based on data in the latch;
  - a compare circuit, connected to the error word generator and the edit portion of the edit buffer, for generating an error signal based on the error word and the error correction word in the error portion of the edit buffer;
  - a first data bus, connecting the input of the error word generator to the data portion of the edit buffer; and
  - a second data bus, connecting the data portion of the edit buffer to an output latch and connecting the output latch to the first port;
 wherein the edit buffer has an error word port for the error portion and a data word port for the data portion.
2. The error correction system of claim 1, wherein the data portion of the edit buffer comprises a header portion and a raw data portion and wherein the data word port has a header word port for the header portion and a raw word port for the raw word portion.
3. The error correction system of claim 1, wherein the data portion of the edit buffer comprises a header portion and a prepend data and postpend data portion and wherein the data word port has a header word port for the header portion and a prepend and postpend data port for the prepend data and postpend data.

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activating the data buffer outputs to modulate charge on the plurality of data bus lines;

waiting for a sufficient time for the plurality of data bus lines to develop a charge differential;

latching the plurality of data bus lines on the data latch; and

performing a cyclical redundancy check on data latched by the data latch.

9. A method for performing multiple operations in a single cycle in a cyclical redundancy check system, the system having a port, an input buffer, an input latch, a first data bus, a register, an output latch, and a second data bus, the method comprising the steps of:

activating the input buffer to receive data from the port;

latching data from the input buffer into the input latch;

disabling the input buffer;

transmitting data on the input latch to the first data bus; and

activating the output latch to transfer the contents of the second data bus to the port.

10. The method of claim 9, further comprising the steps of:

storing data on the first data bus in the register, and

processing data stored in the register.

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